REMARKS

Claims 1-34 are pending in the application

The Examiner objects to claim 12 for a variety of informalities.

The Examiner rejects claims 1-8, 10-15, and 21-26 under 35 U.S.C. §102(b) as being anticipated by Ishibashi et al. (U.S. Patent No. 5,621,774).

The Examiner rejects claims 9, 16-20, and 27 under 35 U.S.C. §103(a) as being unpatentable over Ishibashi in view of Bedell et al. (U.S. Patent No. 5,734,685).

The Examiner rejects claims 28-34 under 35 U.S.C. §103(a) as being unpatentable over Ishibashi in view of Bedell.

Applicants amend claim 12.

Claims 1-34 remain in the case.

Applicants add no new matter and request reconsideration.

Claim Objections

Applicants amend claim 12 to obviate the Examiner's objections. More specifically, Applicants replace "date" with —data— as suggested by the Examiner.

Claim Rejections Under § 102(b)

The Examiner rejects claims 1-8, 10-15, and 21-26 under 35 U.S.C. §102(b) as being anticipated by Ishibashi. Applicants respectfully traverse the rejection.

Claim 1 recites *a signal generator coupled to receive a reference signal, said signal generator generating said latching control signals based upon said reference signal.* Claim 21 recites a similar limitation. According to the Examiner, Ishibashi's variable delay circuit 11 discloses the recited signal generator. Variable delay circuit 11, however, does not *generate* any control signals, as it only delays and transfers an input clock signal CK to latch circuits Lin(0)-Lin(n). Ishibashi, figures 1A, 4A, and 4B; col. 4, lines 7-12. Since, variable delay circuit 11 does not *generate* latching control signals, Ishibashi does not disclose the recited signal generator. Ishibashi, therefore, does not anticipate claim 1, or claim 21, and their corresponding dependent claims.

Claim 1 further recites *an adjustable delay element coupled to receive a clock signal and delaying said clock signal by a variable delay to derive said reference signal.* According to the Examiner, one of Ishibashi's delay circuits DL(1)-DL(a) within variable delay circuit 11 discloses the recited adjustable delay element. Delay circuits DL(1)-DL(a), however, each have a "predetermined amount of delay" and thus the amount of delay is not *variable*.

Ishibashi, col. 4, lines 17-19; col. 5, lines 6-16. The Examiner's assertion falls short since the delay circuits DL(1)-DL(a) (or variable delay circuit 11 for that matter) do not derive a reference signal that is input to variable delay circuit 11 (the Examiner identified delay circuit 11 as disclosing the recited signal generator). Ishibashi, figure 1A; col. 4, lines 7-12. Ishibashi, therefore, does not anticipate claim 1 or its corresponding dependent claims.

Claim 1 further recites *each of said latching control signals coincides approximately with a midpoint of a data period.* Claims 21 and 28 recite a similar limitation. Ishibashi does not disclose this feature. Ishibashi discloses setting a received clock signal to the center of a valid area where all of the received data DT(0)-DT(n) can be latched, but not necessarily latching any data unit at *approximately the midpoint of their corresponding data period.* Ishibashi, figures 15 and 16; col. 8, lines 16-56. Since Ishibashi does not teach latching a data unit at the midpoint of their corresponding data period, Ishibashi does not anticipate claim 1, or claims 21 and 28, and their corresponding dependent claims.

Claim 5 recites *a delay control mechanism, said delay control mechanism adjusting said variable delay imposed by said adjustable delay element to alter said reference signal.* The Examiner alleges Ishibashi's variable delay control circuit 52 discloses the recited delay control mechanism. But variable delay control circuit 52 does not adjust a variable delay imposed by delay circuits DL(1)-DL(a), since each delay circuit DL(1)-DL(a) has a "predetermined amount of delay" and thus cannot be *adjusted* as required by the claim. Ishibashi, col. 4, lines 17-19; col. 5, lines 6-16. Since, variable delay control circuit 52 does not adjust the variable delay imposed by the adjustable delay element, Ishibashi does not disclose the recited delay control mechanism. Ishibashi, therefore, does not anticipate claim 5 or its corresponding dependent claims.

Claim 23 recites the *reference signal coincides approximately with a midpoint of a data period.* Claim 31 recites a similar limitation. According to the Examiner, variable delay circuit 11 discloses the recited signal generator that receives the recited reference signal. Even though the Examiner does not specify which signal entering variable delay circuit 11 (CK or SEL) discloses the recited reference signal, neither signal *coincides approximately with a midpoint of a data period.* Ishibashi, col. 4, lines 7-29; col. 8, lines 16-56; figure 1A. Since Ishibashi does not teach a reference signal that coincides approximately with a midpoint of a data period, Ishibashi does not anticipate claim 23, or claim 31, and their corresponding dependent claims.

Claim Rejections Under § 103(a)

The Examiner rejects claims 9, 16-20, 27-34 under 35 U.S.C. §103(a) as being unpatentable over Ishibashi in view of Bedell. Applicants respectfully traverse the rejection.

Claim 28 recites *a delay locked loop coupled to receive a reference signal, said delay locked loop generating said latching control signals based upon said reference signal such that each of said latching control signals coincides approximately with a midpoint of a data period.* Claims 9, 16 and 27 recite similar limitations. According to the Examiner, Bedell's deskewing circuit 15 discloses the recited delay locked loop. Deskewing circuit 15, however, does not *generate* any control signals, as it delays and transfers the input clock signal to a predetermined phase. Bedell, figures 1, 2, and 3; col. 5, line 38 – col. 6, line 20. Since, deskewing circuit 15 does *generate* latching control signals, Bedell does not disclose the recited delay locked loop. The combination of Ishibashi and Bedell, therefore, cannot obviate claim 28, or claims 9, 16 and 27, and their corresponding dependent claims.

And neither Ishibashi nor Bedell provide any motivation to combine the inventions described therein. The Examiner alleges since "a delay locked loop generating said latching control signals based upon said reference signal is a well-known technique introduced in many references," that "[i]t would have been obvious for one skilled in the art" to have been motivated "to apply the method as taught by Bedell et al. to modify the invention of Ishibashi et al. since it is well known in the art to use either phase-locked loop or delay locked loop techniques to adjust delays on non-clock signal paths." Office Action, page 9. This combination, however, would not have provided motivation for using a deskewing circuit to adjust delays since Bedell does not adjust delays in received signals, but aligns a clock signal CLKL and its corresponding data signal DATL to a predetermined phase. Bedell, figures 1, 2, and 3; col. 5, line 38 – col. 6, line 20. In other words, since Ishibashi realigns data, that has been randomly misaligned during transmission to the receiver, by dynamically delaying a clock signal, there would be no motivation to use Bedell's predetermined clock alignment. Bedell, further, aligns multiple spatially separated data signals DATL(1)-DATL(N) to a single predetermined phase *without a latching mechanism*. Bedell, figure 2; col. 5, line 38 – col. 6, line 20. Thus, there would be no motivation to combine Bedell's data realignment with Ishibashi's latching system. Thus combining the references, as the Examiner suggests, is to no avail.

CONCLUSION

For the foregoing reasons, the Applicant requests reconsideration and allowance of all claims as amended. The Applicant encourages the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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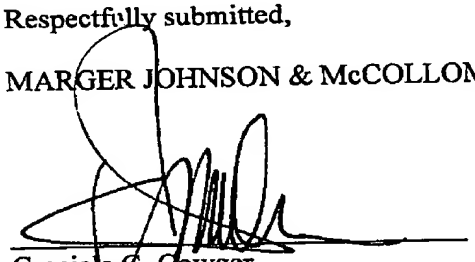

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